Hyperspectral Processing Using FPGAs and DSPs

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As focal plane technology advances, it becomes increasingly practical to reduce the size and increase the portability of remote sensing instruments. To achieve smaller and more portable instruments, supporting electronics hardware and computing elements must similarly decrease in size, weight, and power consumption, while also increase in computing ability to meet new real-time processing needs. To meet the packaging, power, and processing (P3) requirements, real-time processing systems will need to be assembled using combinations of FPGAs and DSP processors rather than bulky, expensive, and less efficient general purpose computing devices. Smaller instruments with real-time feedback will increase the portability, range and value for many of the Laboratory's customers.

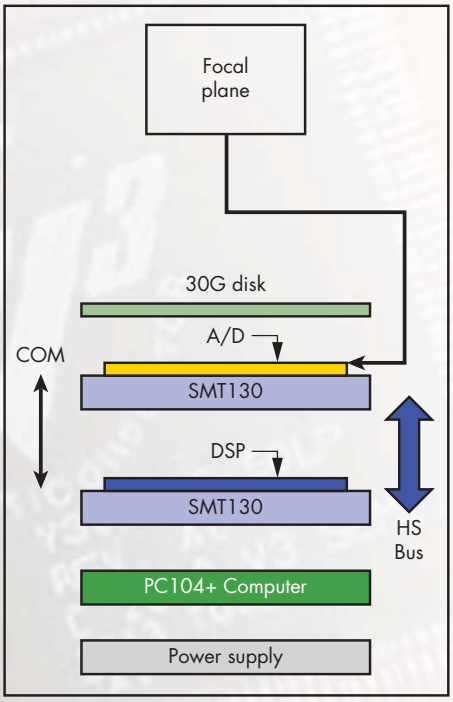

Figure 1. Functional block diagram of hyperspectral embedded processing system.

Project Goals

Our goals are to evaluate the processing requirements to perform covariance estimation, eigenfactorization, and matched filtering (L3 processing) hyperspectral data processing; to build a controller to archive data and operate the A/D and DSP components using a single board computer; to build a prototype to digitize at least four channels of analog information clocked off a hyperspectral focal-plane array, and process the data prior to L3 by performing bad-pixel correction and spectral calibration (L1 processing); build a prototype that performs real-time hyperspectral data processing from a complete data cube, through one or more algorithms selected from the L1 and L3 processing chains (Fig. 1).

Relevance to LLNL Mission

This project will provide the Laboratory with engineering experience in small-scale, low-power, low-cost, real-time processing systems for hyperspectral

imagery that can be extended to any complex mathematical problem where P3 requirements are key.

FY2004 Accomplishments and Results

Our major milestones include the following: all algorithms have been identified and coded in C; covariance estimation, eigenfactorization, and L3 processing have been implemented; all hardware and software for engineering the final configuration have been acquired and tested (see Figs. 2 and 3 for examples); packaging has been assembled; and spectral calibration and L1 processing have been synthesized for the Xilinx Virtex II FPGA. Portions of those algorithms have been tested and are being assembled for system verification and performance metrics.

Related References

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4. Jaenick, A., and W. Luk, "Parameterised Floating-Point Arithmetic on FPGAs," *IEEE International Conference on Acoustics, Speech, and Signal Processing Proceedings*, 2001.
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FY2005 Proposed Work

While the DSP board can perform L3 processing and the A/D board can digitize and perform L1 processing, the data path between the boards is marginal. Additionally, the L3 processing must be optimized. The covariance estimation is particularly intensive due to the number of memory read/writes. Therefore, the FPGA on the DSP board will be used to either calculate the covariance or provide a buffer/pre-fetch area to mitigate the poor performance reading/writing from memory. We will optimize the L3 processing and the data pathways from analog signal to bytes on disk.

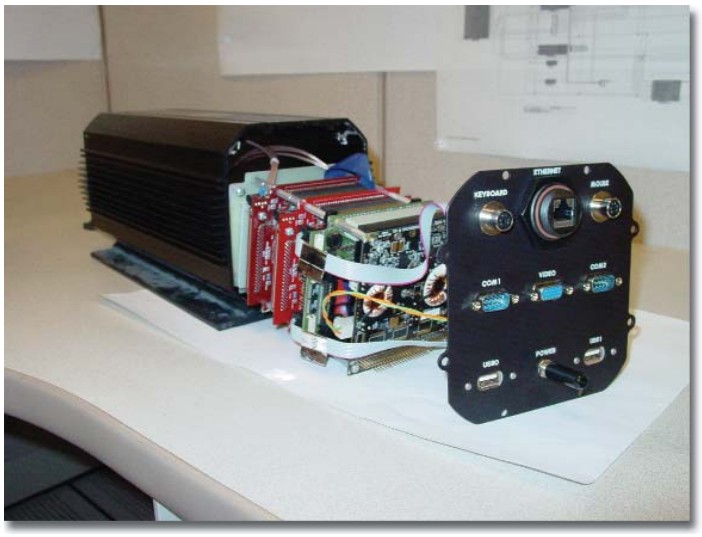

Figure 2. Hardware implementation for hyperspectral embedded processing system.

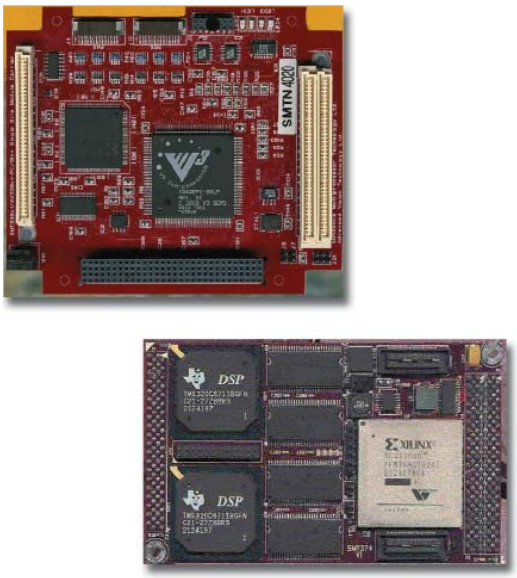

Figure 3. Sundance PC-104+ carrier board (top) and Sundance dual TI 6713 DSP module (bottom).